Fig. 1

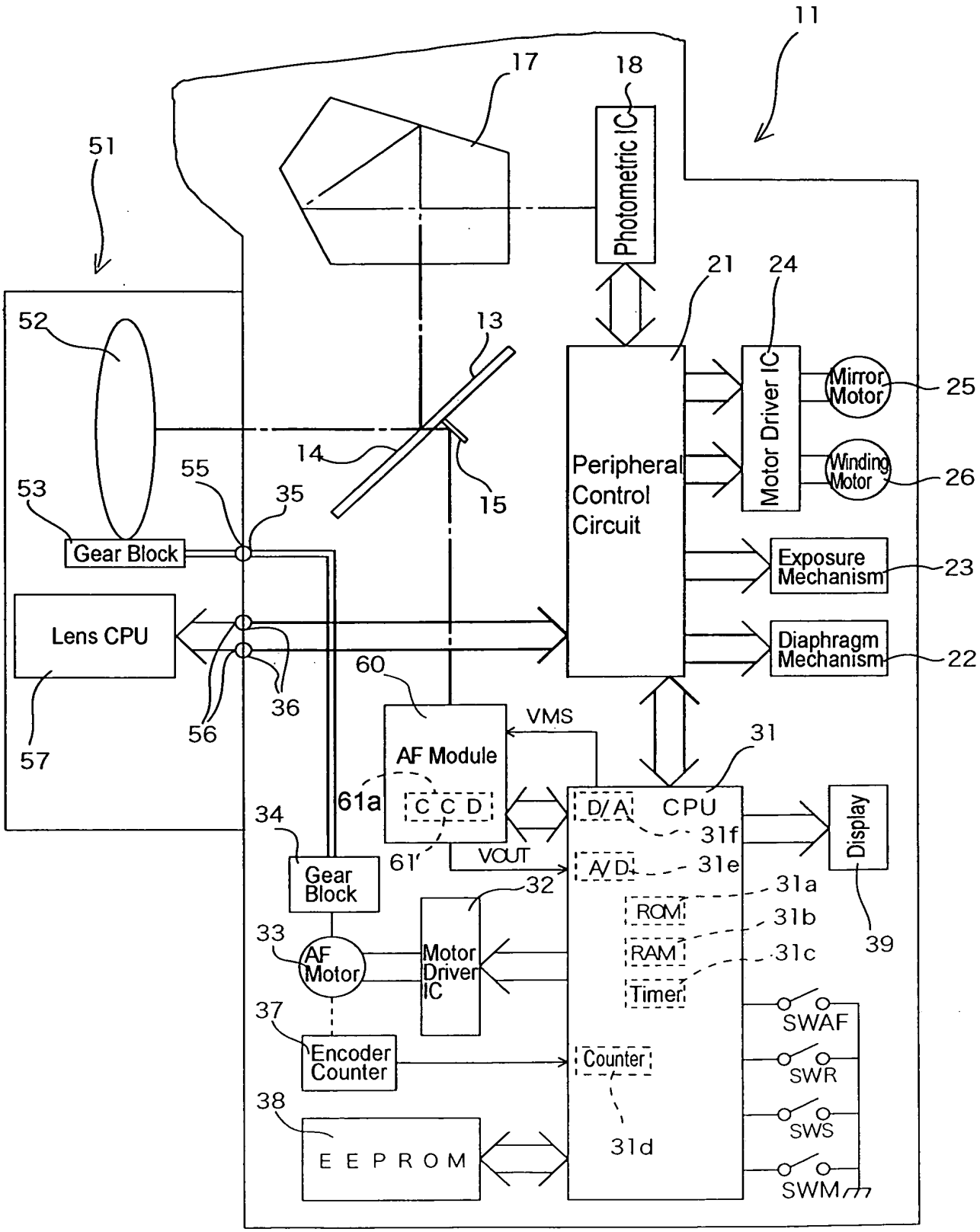
11
17
18
Photometric IC
51
52
13
14
15
53
55
35
Gear Block
Lens CPU
57
56
36
21
24
Peripheral Control Circuit
Motor Driver IC
Mirror Motor
25
Winding Motor
26
Exposure Mechanism
23
Diaphragm Mechanism
22
60
VMS
AF Module
61a
C C D
61'
VOUT
31
D/A
CPU
31f
A/D
31e
31a
ROM
31b
RAM
31c
Timer
Display
39
34
Gear Block
32
33
AF Motor
Motor Driver IC
37
Encoder Counter
Counter
31d
38
E E P R O M
SWAF
SWR
SWS
SWM

Fig. 2

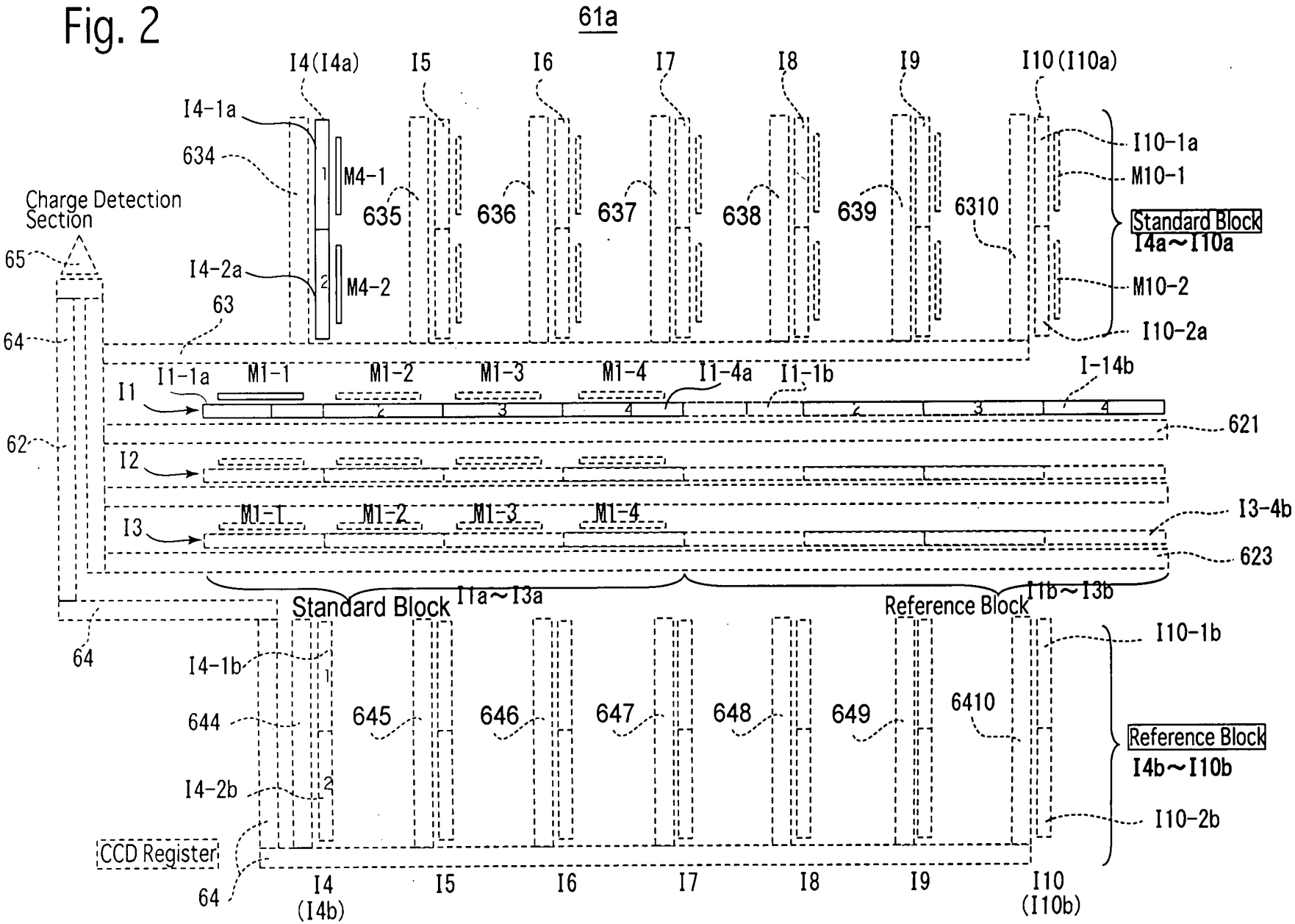
61a
I4(I4a)
I5
I6
I7
I8
I9
I10(I10a)
I4-1a
634
M4-1
635
636
637
638
639
6310
I10-1a
M10-1
Standard Block
I4a~I10a
M10-2
I10-2a
Charge Detection Section
65
I4-2a
M4-2
63
64
I1-1a
M1-1
M1-2
M1-3
M1-4
I1-4a
I1-1b
I-14b
I1
621
62
I2
I3-4b
I3
623
Standard Block
I1a~I3a
Reference Block
I1b~I3b
64
I4-1b
I10-1b
644
645
646
647
648
649
6410
Reference Block
I4b~I10b
I4-2b
I10-2b
CCD Register
64
I4
(I4b)
I5
I6
I7
I8
I9
I10
(I10b)

Fig. 3

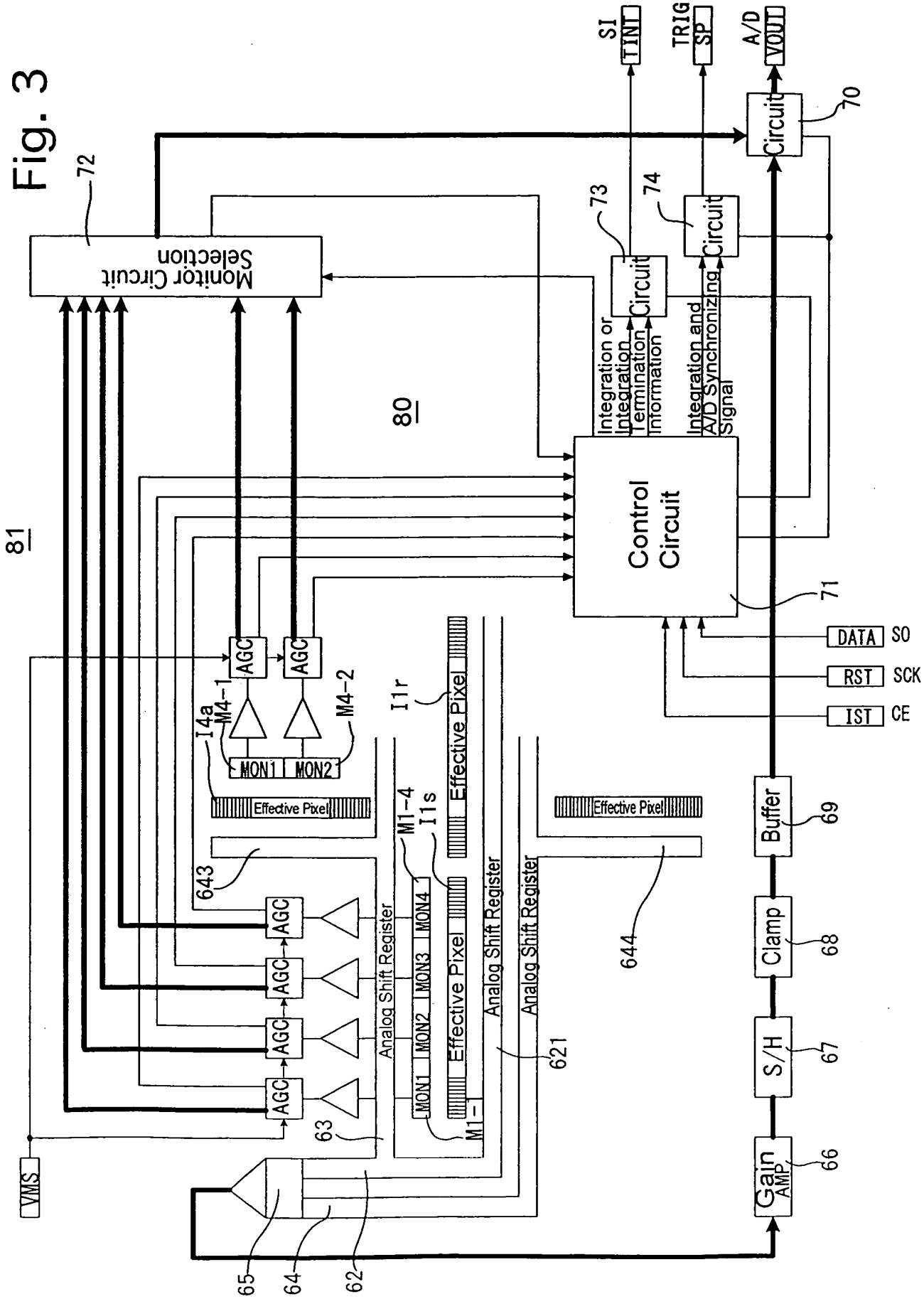
81
80
72
Monitor Circuit Selection
Control Circuit
71
70
Circuit
73
74
Integration or Integration Termination Information
Integration and A/D Synchronizing Signal
SI
TINT
TRIG
SP
A/D
VOUT
DATA
SO
RST
SCK
IST
CE
AGC
M4-1
M4-2
14a
I1r
I1s
M1-4
M1-
MON1
MON2
MON3
MON4
Effective Pixel
Analog Shift Register
643
644
621
63
65
64
62
VMS
Buffer
69
Clamp
68
S/H
67
Gain AMP
66

Fig. 4

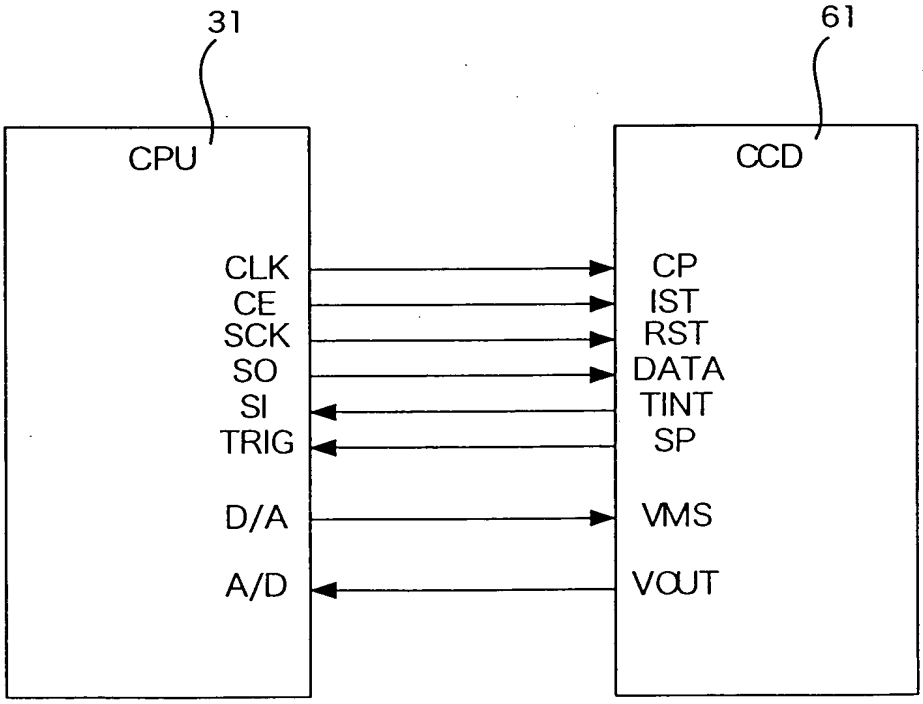
31
61
CPU
CCD
CLK
CE
SCK
SO
SI
TRIG
D/A
A/D
CP
IST
RST
DATA
TINT
SP
VMS
VOUT

Fig. 5

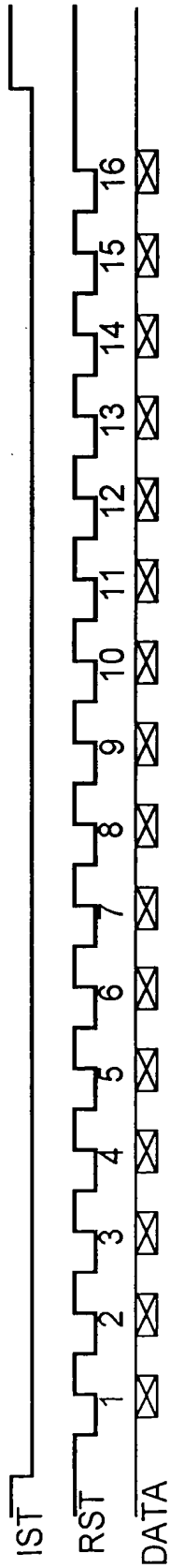

Fig. 6

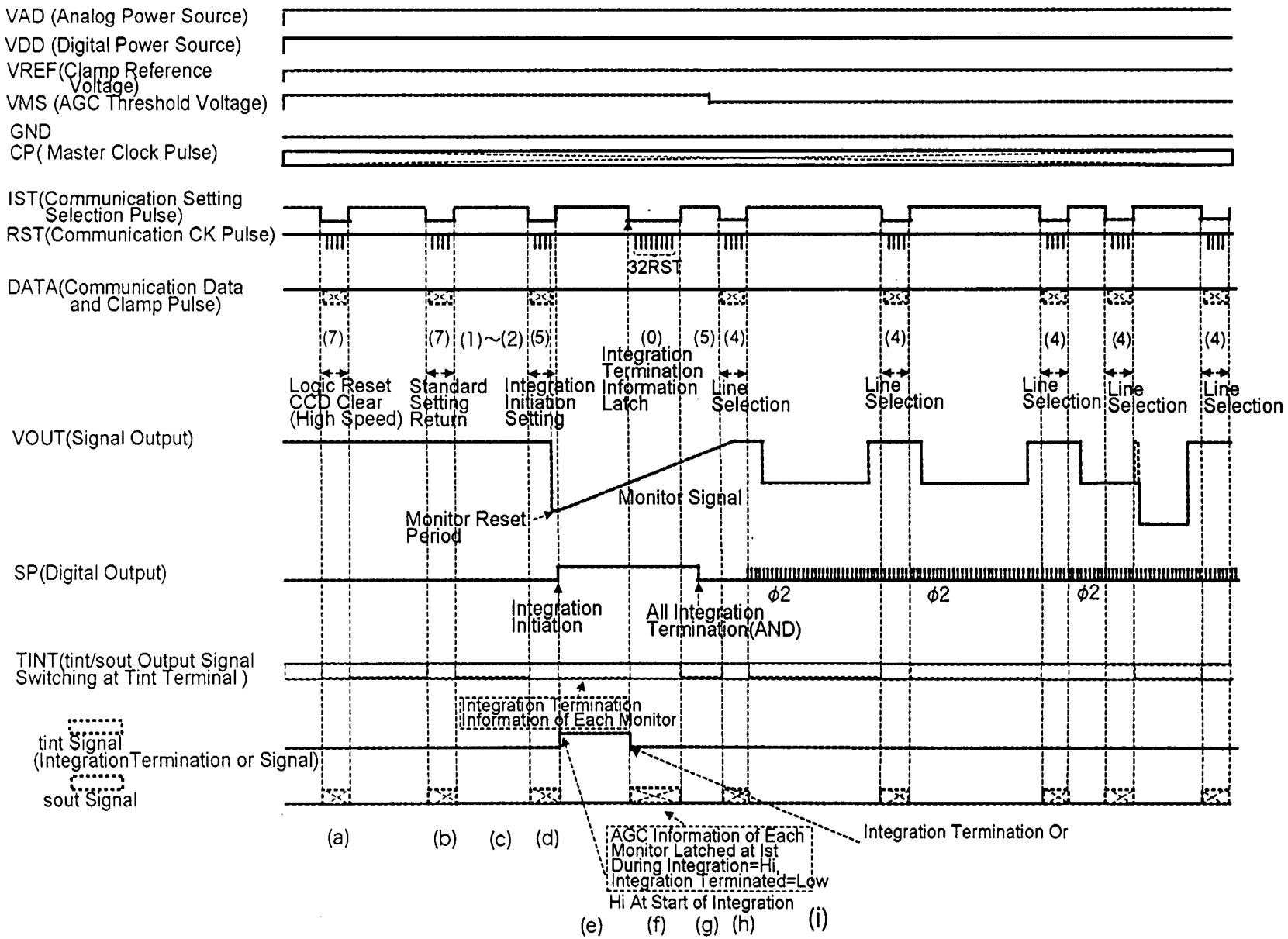
VAD (Analog Power Source)
VDD (Digital Power Source)
VREF(Clamp Reference Voltage)
VMS (AGC Threshold Voltage)
GND
CP(Master Clock Pulse)
IST(Communication Setting Selection Pulse)
RST(Communication CK Pulse)
DATA(Communication Data and Clamp Pulse)
32RST
(7)
(7)
(1)~(2)
(5)
(0)
(5)
(4)
(4)
(4)
(4)
(4)
Logic Reset CCD Clear (High Speed)
Standard Setting Return
Integration Initiation Setting
Integration Termination Information Latch
Line Selection
Line Selection
Line Selection
Line Selection
Line Selection
VOUT(Signal Output)
Monitor Signal
Monitor Reset Period
SP(Digital Output)
Integration Initiation
All Integration Termination(AND)
ϕ2
ϕ2
ϕ2
TINT(tint/sout Output Signal Switching at Tint Terminal)
Integration Termination Information of Each Monitor
tint Signal (IntegrationTermination or Signal)
sout Signal
(a)
(b)
(c)
(d)
AGC Information of Each Monitor Latched at Ist During Integration=Hi, Integration Terminated=Low
Integration Termination Or
Hi At Start of Integration
(e)
(f)
(g)
(h)
(i)

Fig. 7

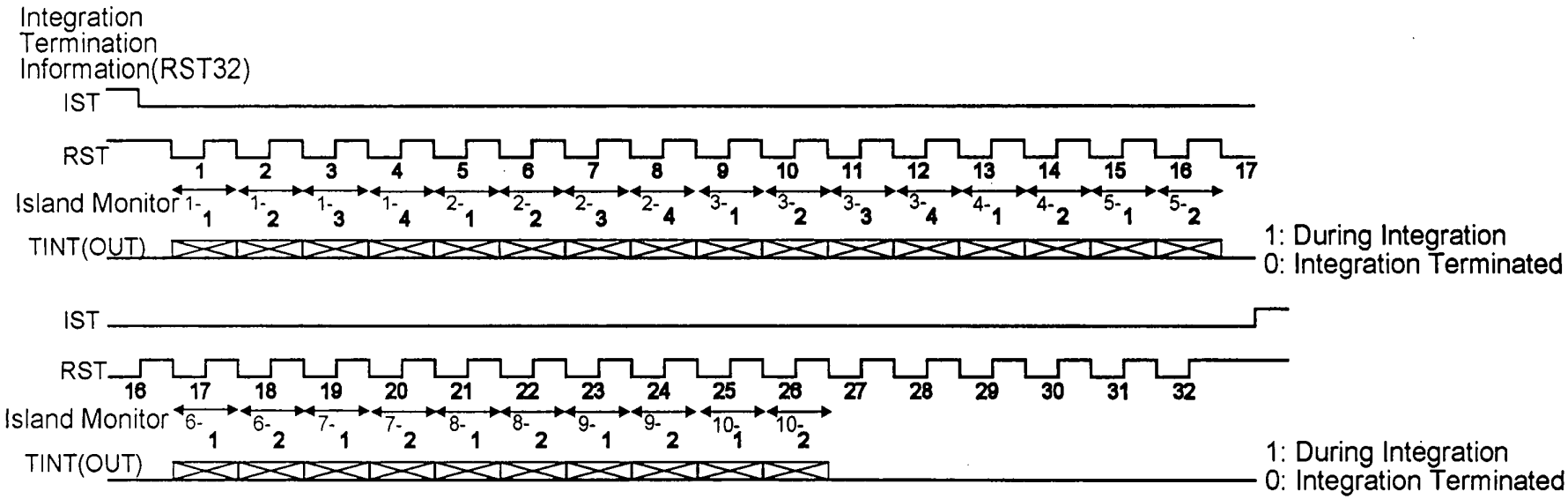
Integration
Termination
Information(RST32)
IST
RST
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
Island Monitor
1-1 1-2 1-3 1-4 2-1 2-2 2-3 2-4 3-1 3-2 3-3 3-4 4-1 4-2 5-1 5-2
TINT(OUT)
1: During Integration
0: Integration Terminated
IST
RST
16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
Island Monitor
6-1 6-2 7-1 7-2 8-1 8-2 9-1 9-2 10-1 10-2
TINT(OUT)
1: During Integration
0: Integration Terminated

Fig. 8

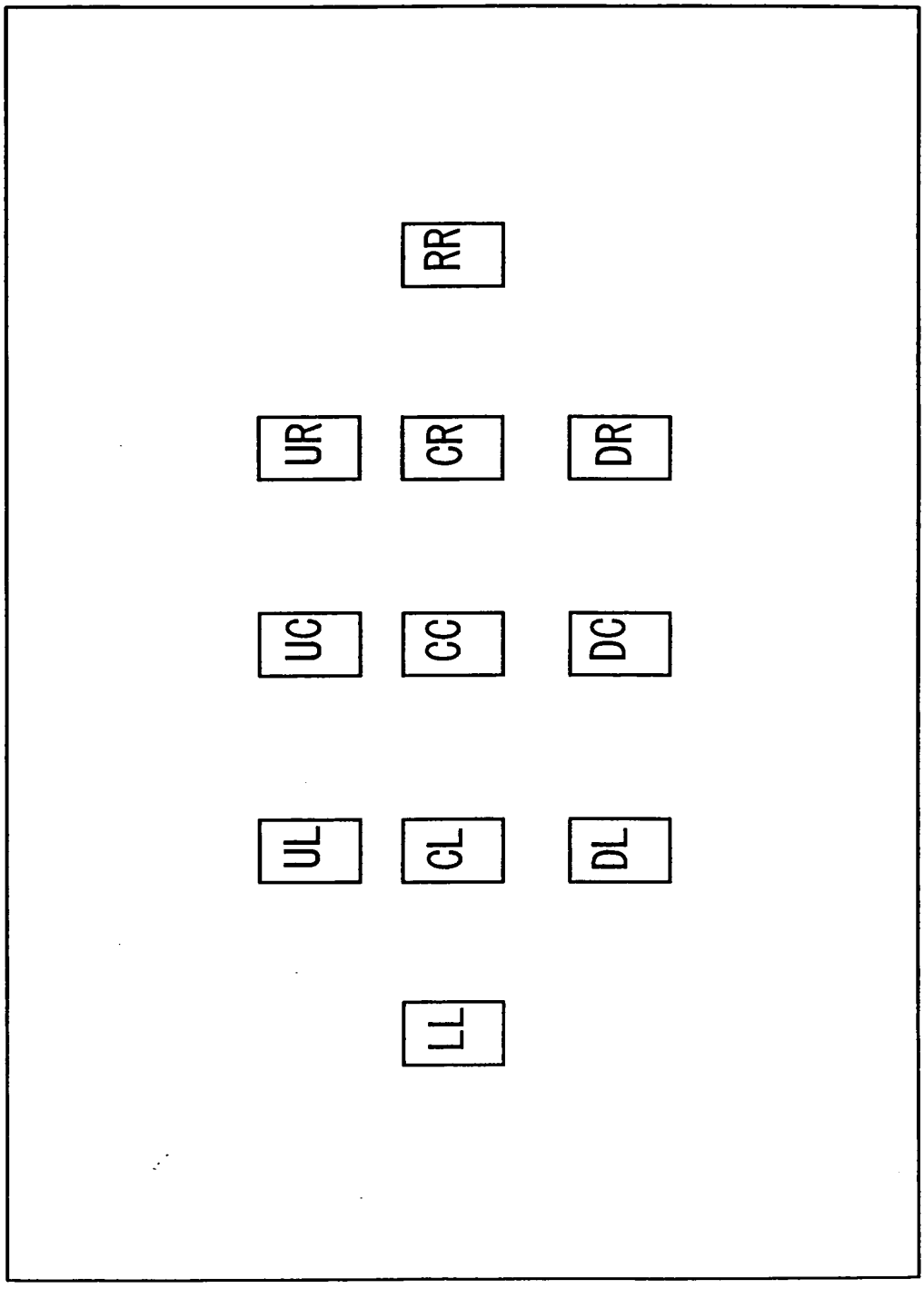

Fig. 9

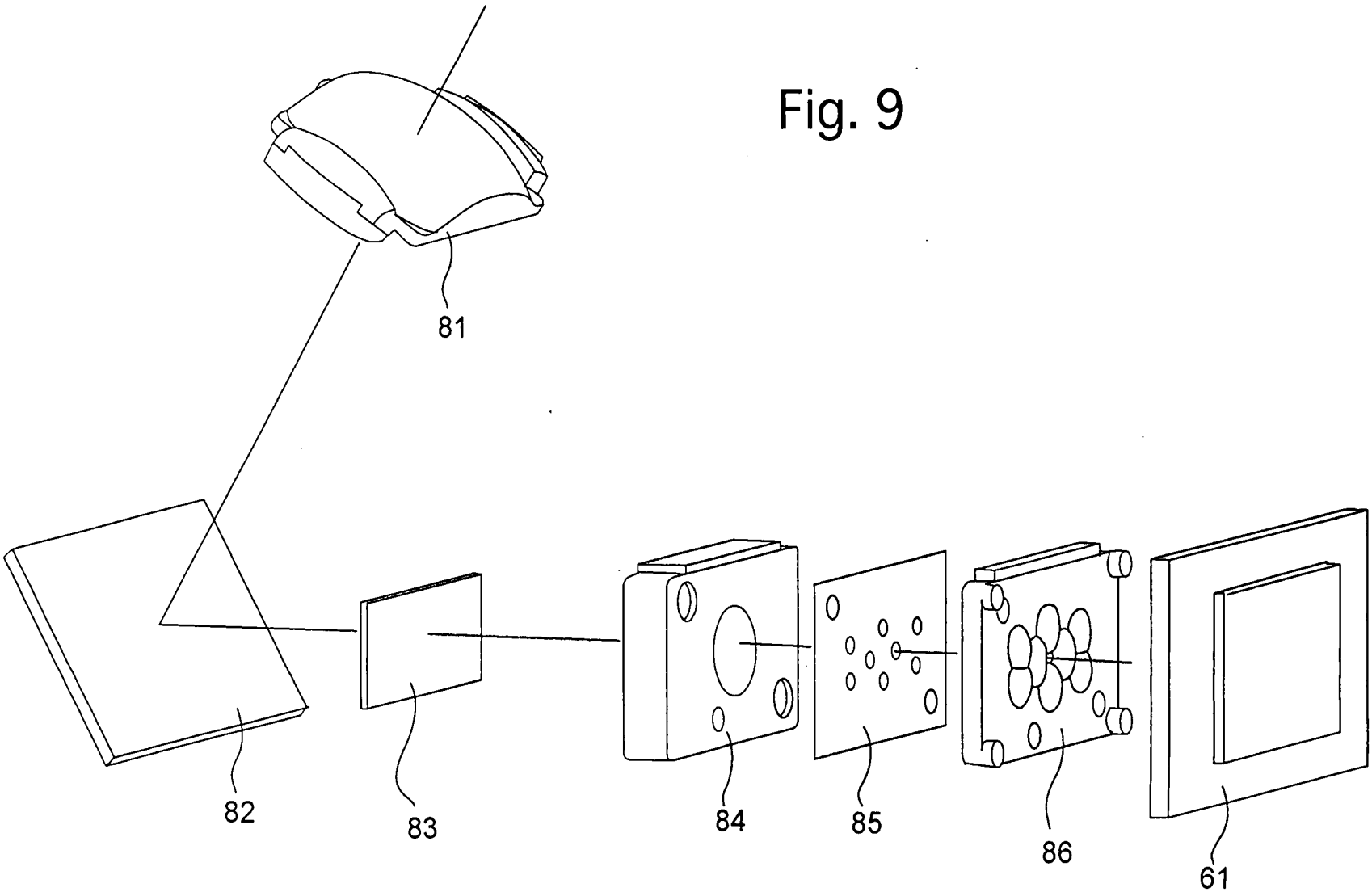

Fig. 10

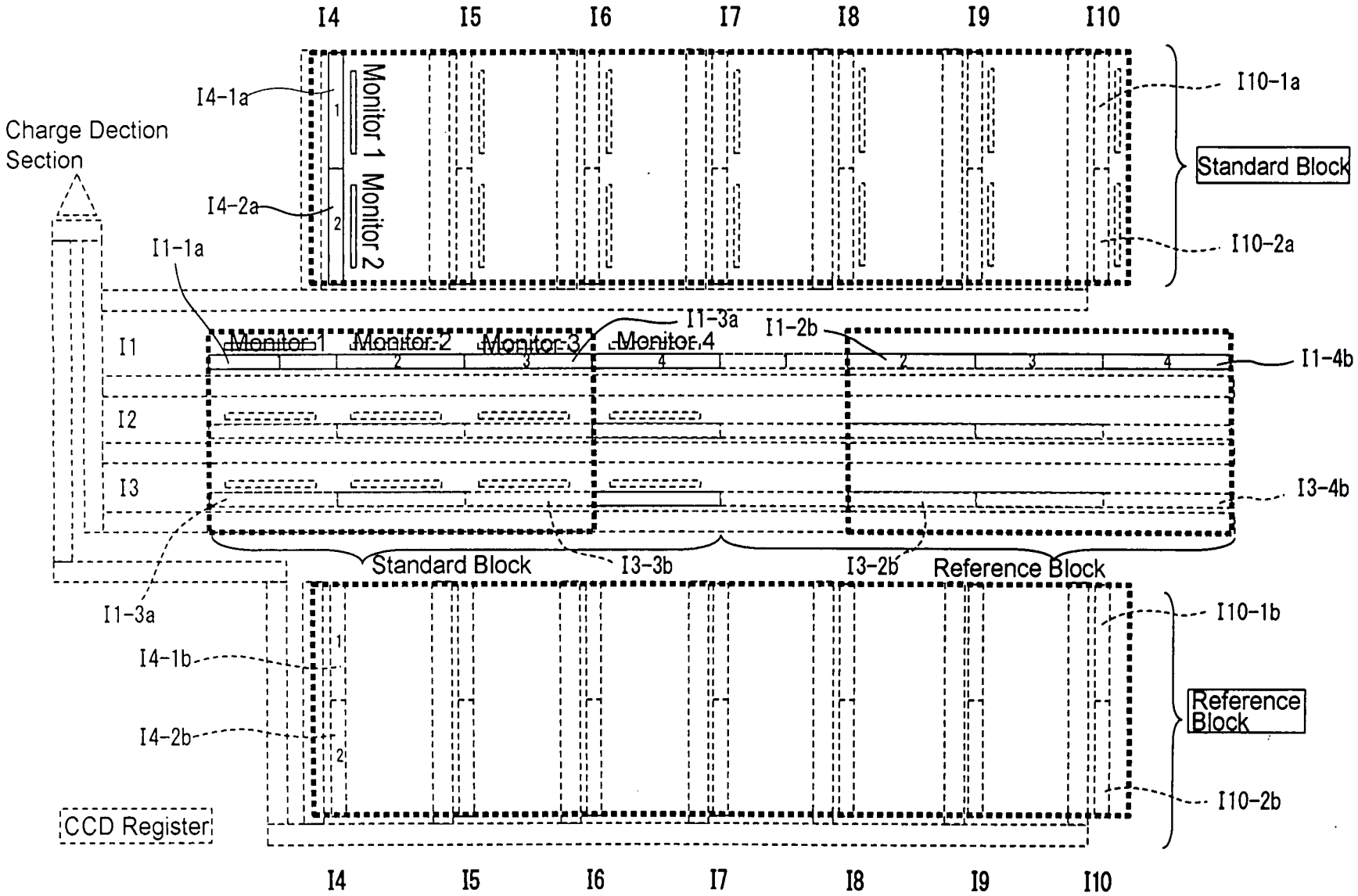
I4
I5
I6
I7
I8
I9
I10
I4-1a
I4-2a
Monitor 1
Monitor 2
Charge Dection Section
I10-1a
Standard Block
I10-2a
I1-1a
I1-3a
I1-2b
I1-4b
Monitor 1
Monitor 2
Monitor 3
Monitor 4
I1
I2
I3
I3-4b
Standard Block
I3-3b
I3-2b
Reference Block
I1-3a
I10-1b
I4-1b
I4-2b
Reference Block
I10-2b
CCD Register
I4
I5
I6
I7
I8
I9
I10

Fig. 11

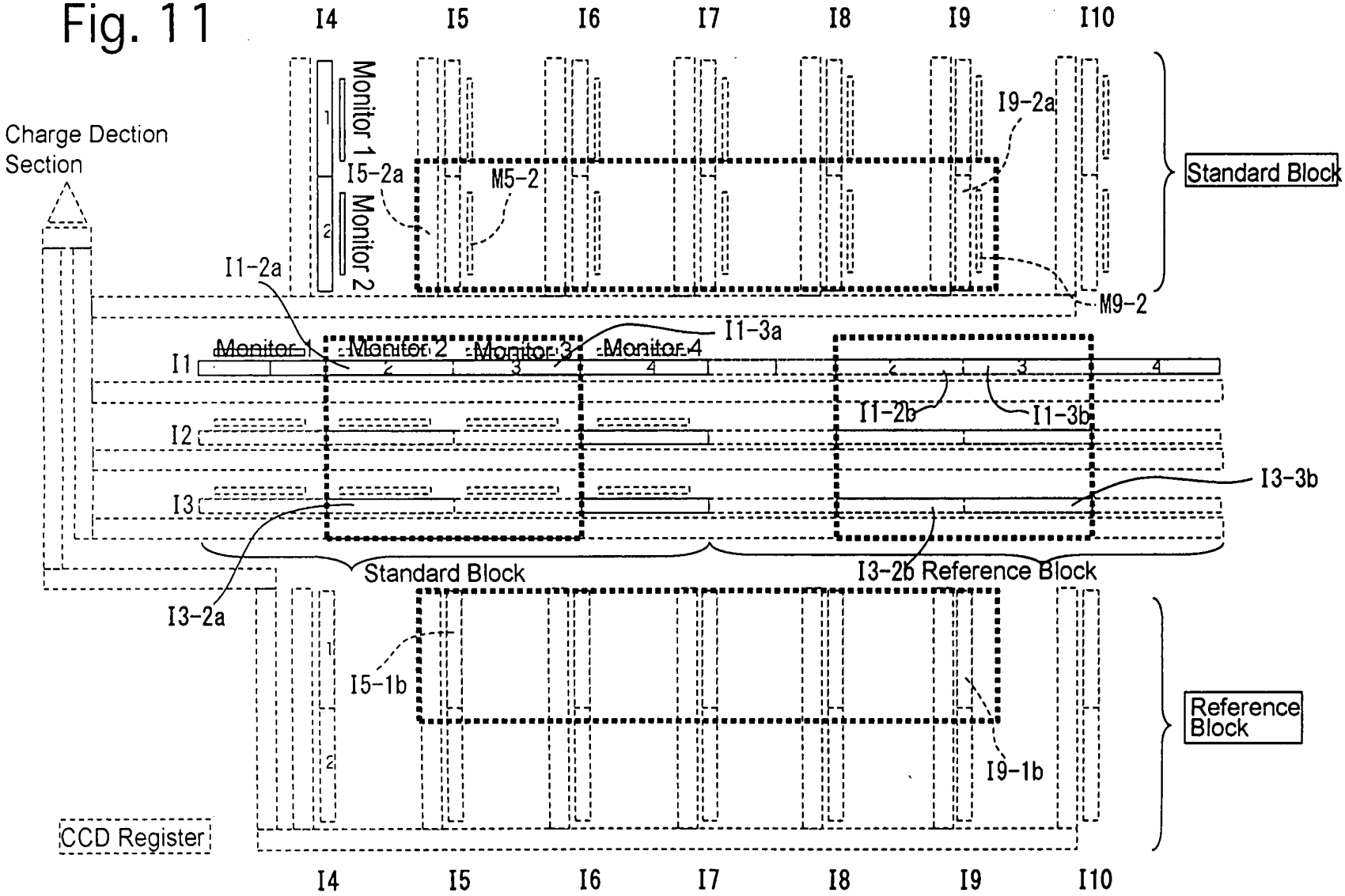
I4
I5
I6
I7
I8
I9
I10
Charge Dection Section
Monitor 1
Monitor 2
I5-2a
M5-2
I9-2a
Standard Block
I1-2a
M9-2
I1-3a
Monitor 1
Monitor 2
Monitor 3
Monitor 4
I1
I2
I3
I1-2b
I1-3b
I3-3b
Standard Block
I3-2b Reference Block
I3-2a
I5-1b
I9-1b
Reference Block
CCD Register
I4
I5
I6
I7
I8
I9
I10

Fig. 12

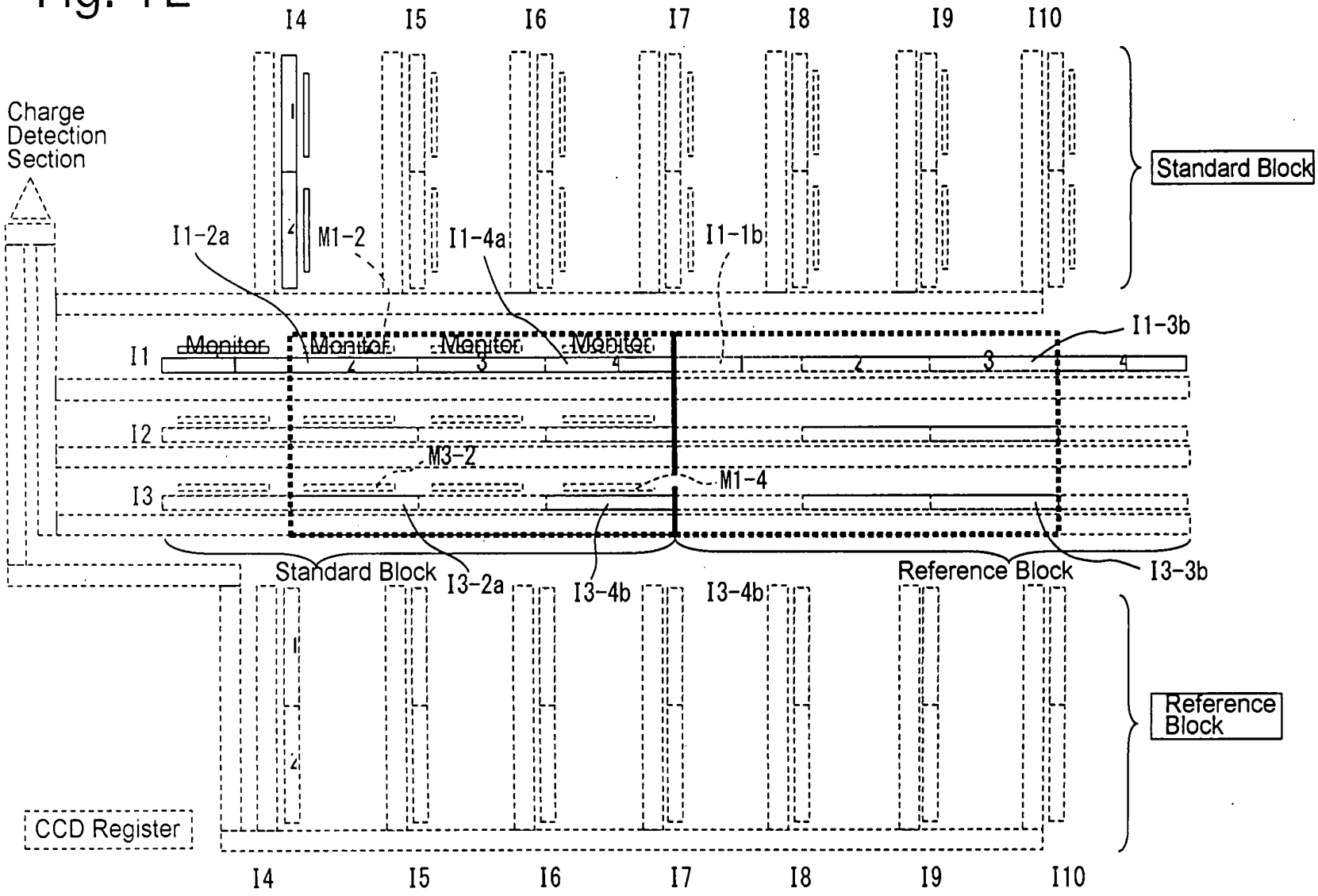
I4
I5
I6
I7
I8
I9
I10
Charge Detection Section
Standard Block
I1-2a
M1-2
I1-4a
I1-1b
I1-3b
I1
Monitor
Monitor
Monitor
Monitor
I2
M3-2
M1-4
I3
Standard Block
I3-2a
I3-4b
I3-4b
Reference Block
I3-3b
Reference Block
CCD Register
I4
I5
I6
I7
I8
I9
I10

Fig. 13

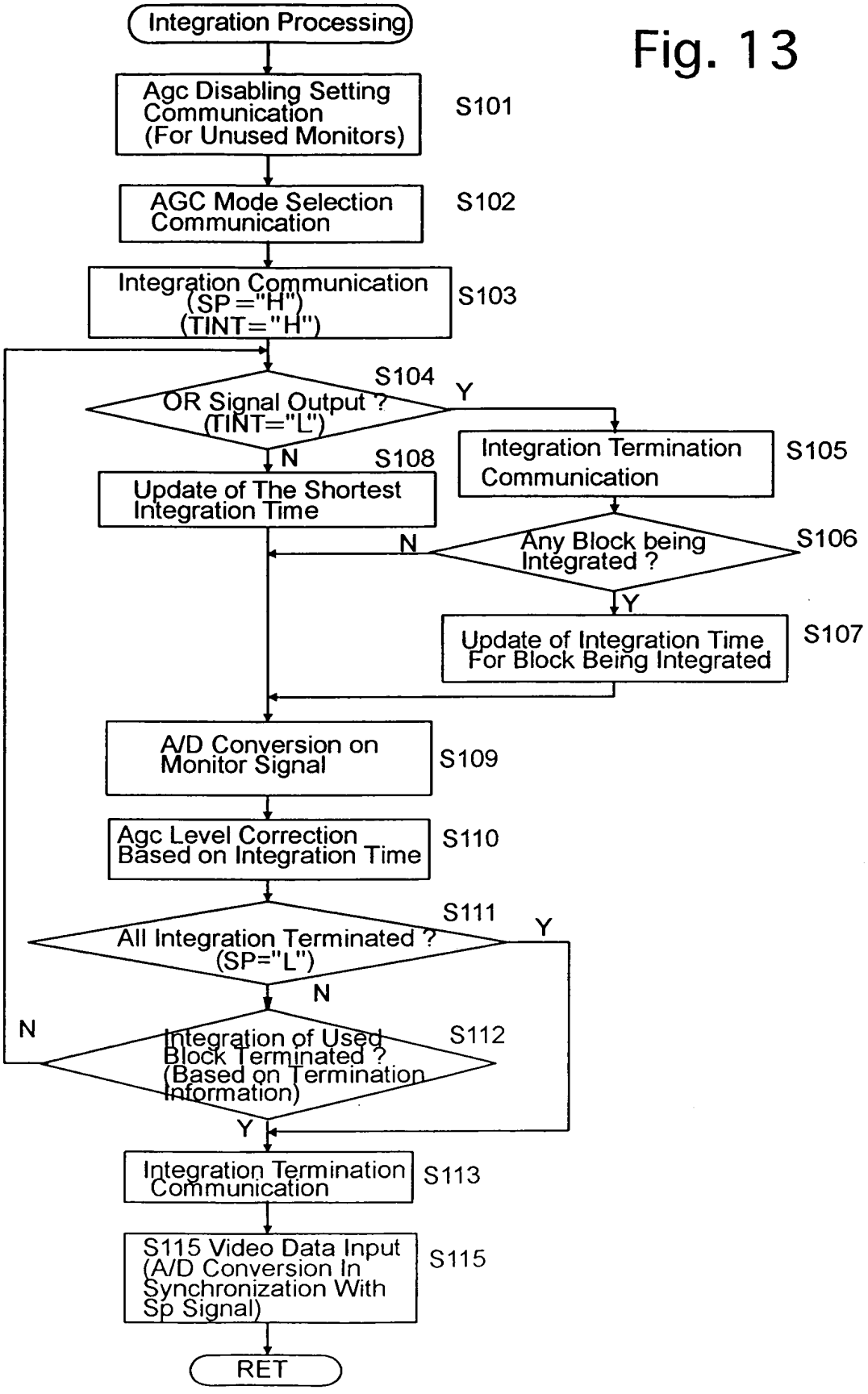
Integration Processing
Agc Disabling Setting Communication (For Unused Monitors)
S101
AGC Mode Selection Communication
S102
Integration Communication (SP="H") (TINT="H")
S103
S104
OR Signal Output ? (TINT="L")
Y
N
S108
Update of The Shortest Integration Time
Integration Termination Communication
S105
Any Block being Integrated ?
S106
N
Y
Update of Integration Time For Block Being Integrated
S107
A/D Conversion on Monitor Signal
S109
Agc Level Correction Based on Integration Time
S110
S111
All Integration Terminated ? (SP="L")
Y
N
N
Integration of Used Block Terminated ? (Based on Termination Information)
S112
Y
Integration Termination Communication
S113
S115 Video Data Input (A/D Conversion In Synchronization With Sp Signal)
S115
RET

Fig. 14

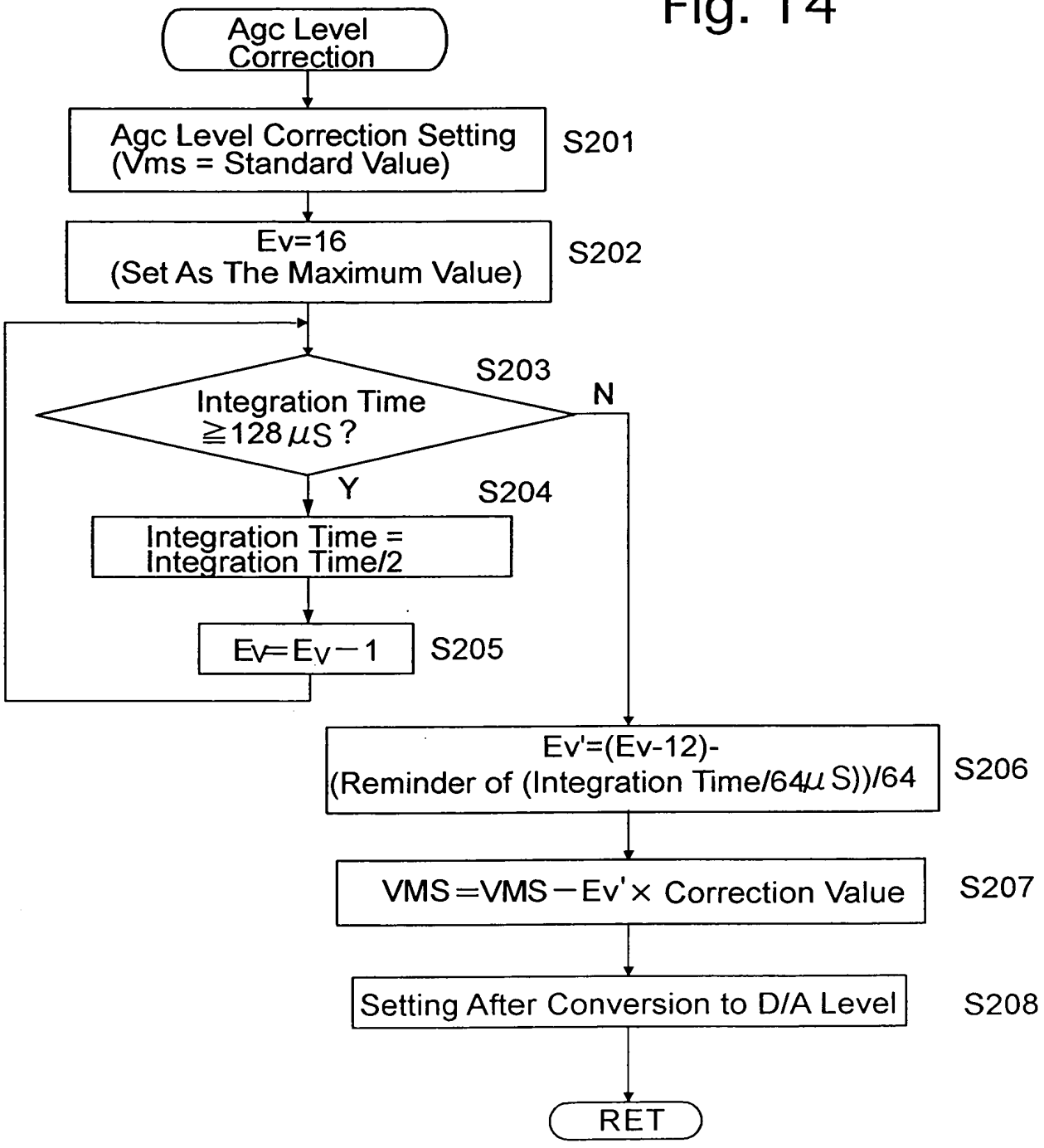
Agc Level Correction
Agc Level Correction Setting (Vms = Standard Value)
S201
Ev=16 (Set As The Maximum Value)
S202
S203
Integration Time ≧128μS ?
N
Y
S204
Integration Time = Integration Time/2
Ev=Ev−1
S205
Ev'=(Ev-12)- (Reminder of (Integration Time/64μS))/64
S206
VMS=VMS−Ev'× Correction Value
S207
Setting After Conversion to D/A Level
S208
RET

Fig. 15A

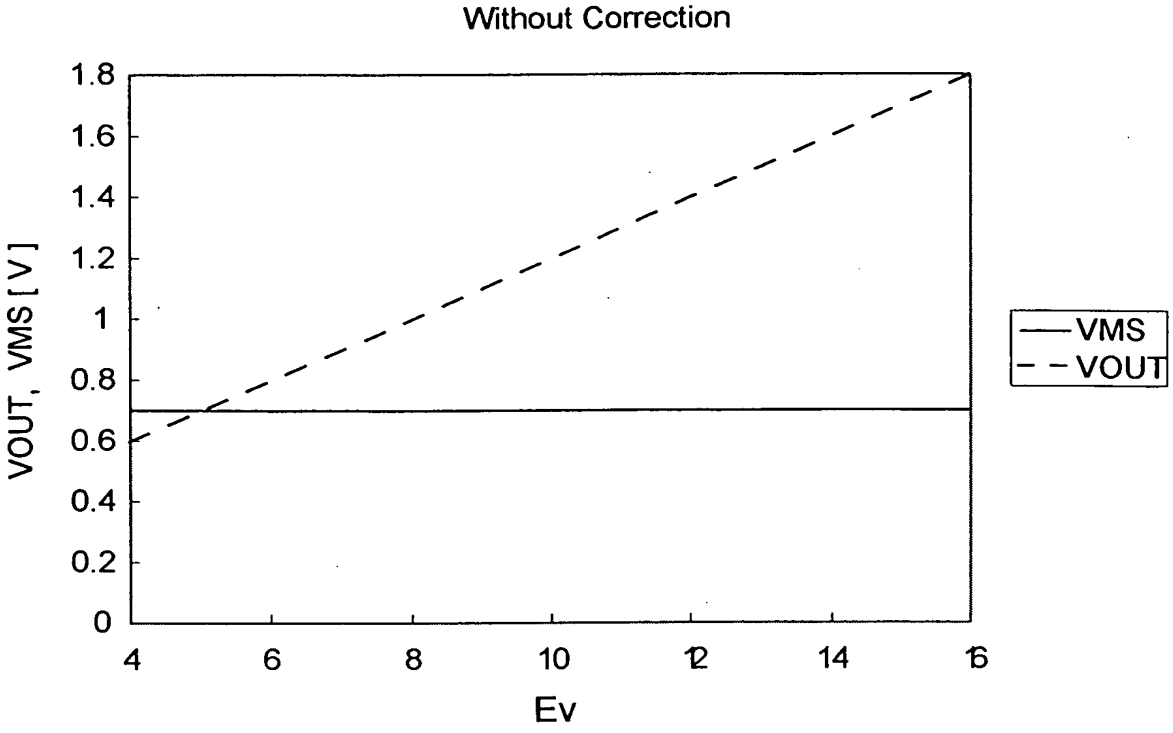

Fig. 15B